DEFECT DETECTION APPROACHES BASED ON SIMULATED REFERENCE IMAGE

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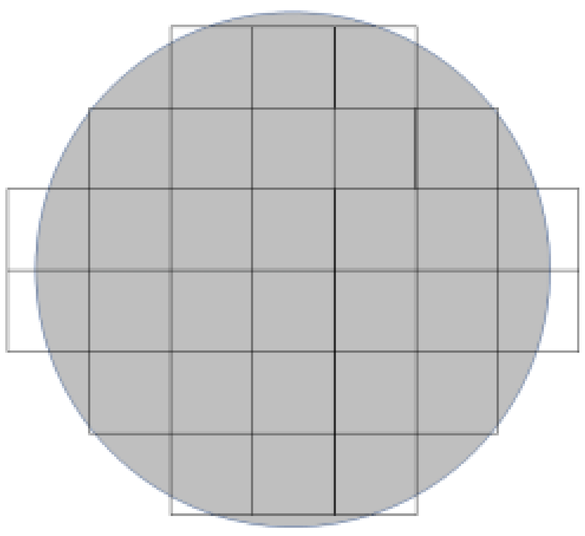
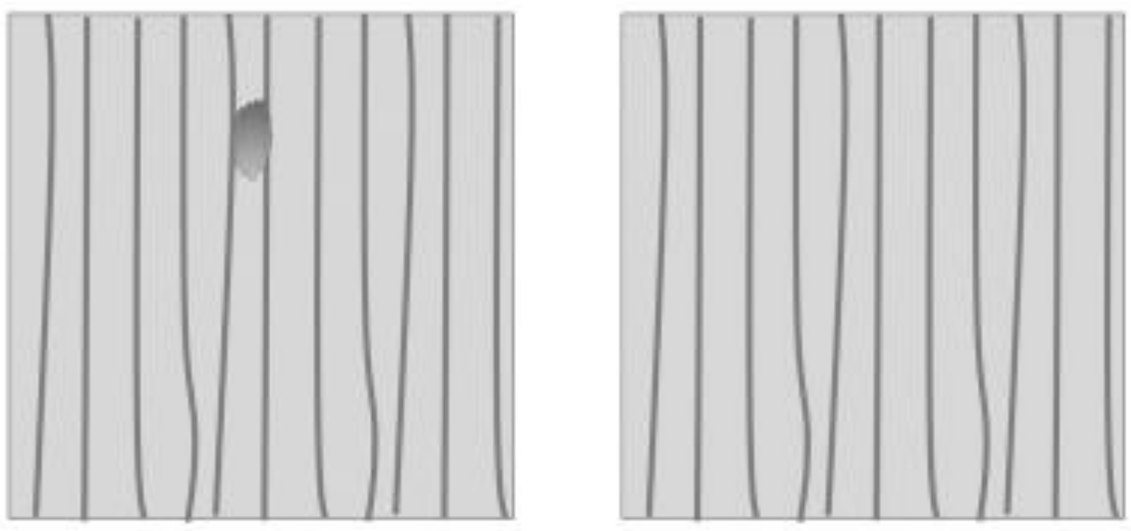
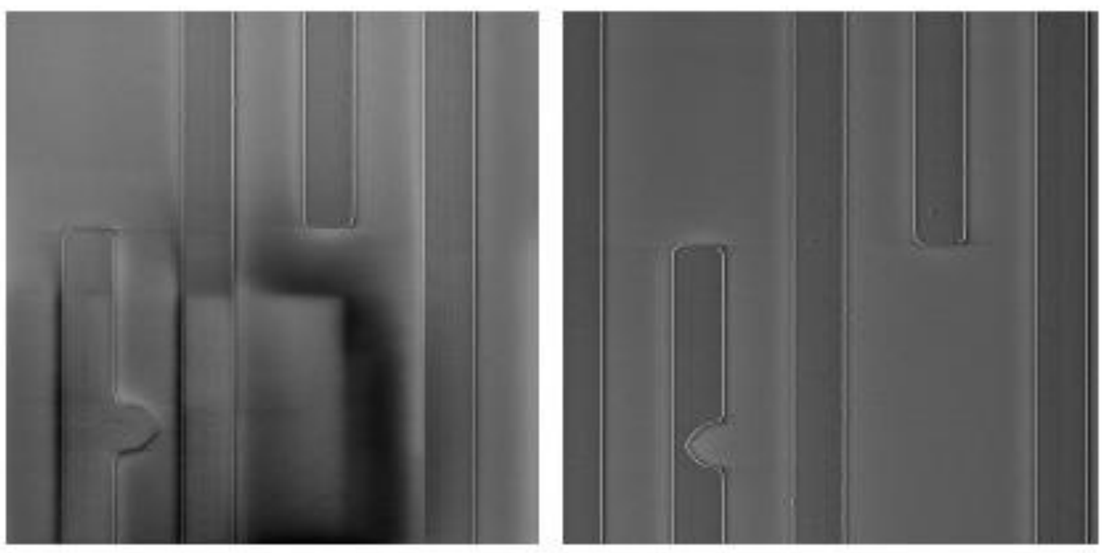
Silicon Wafer:
An illustration of a Silicon wafer and its corresponding dies. A specific die may be a defect candidate, while its corresponding location on another die is its reference clean image. The scanning electron microscopy (SEM) captures a small patch in a specific die such that the nano-meter semiconductor lithography can be seen in high resolution.



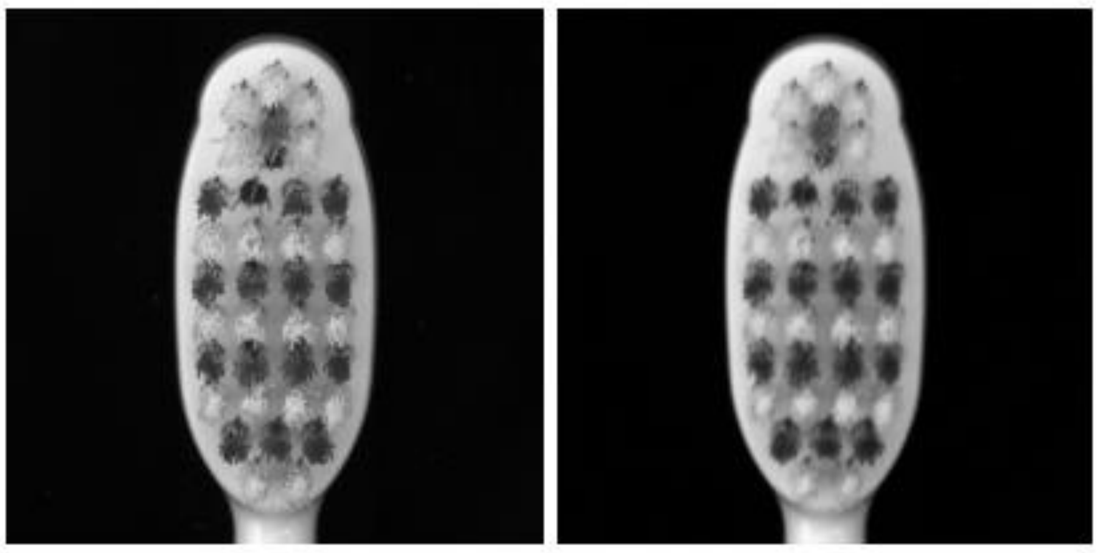
SEM Semiconductor Defects:
Example of a simulation of Scanning-Electron-Microscopy (SEM) image with anomaly and its corresponding clean reference image.



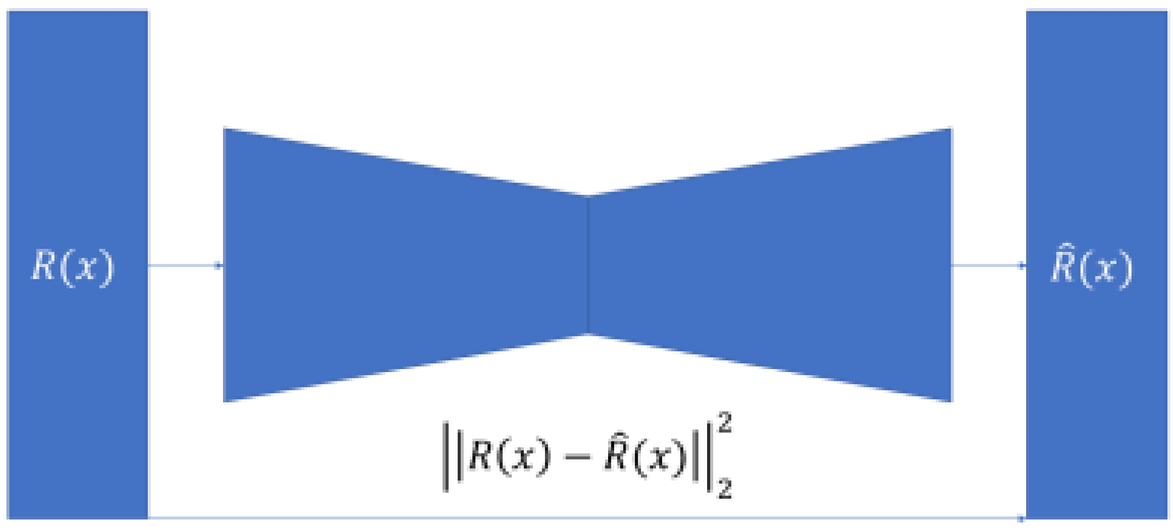
Simulation of SEM Defects:
Simulation of true-defects in SEM images. These specific simulations contain defects which are relatively easy to detect and segment.



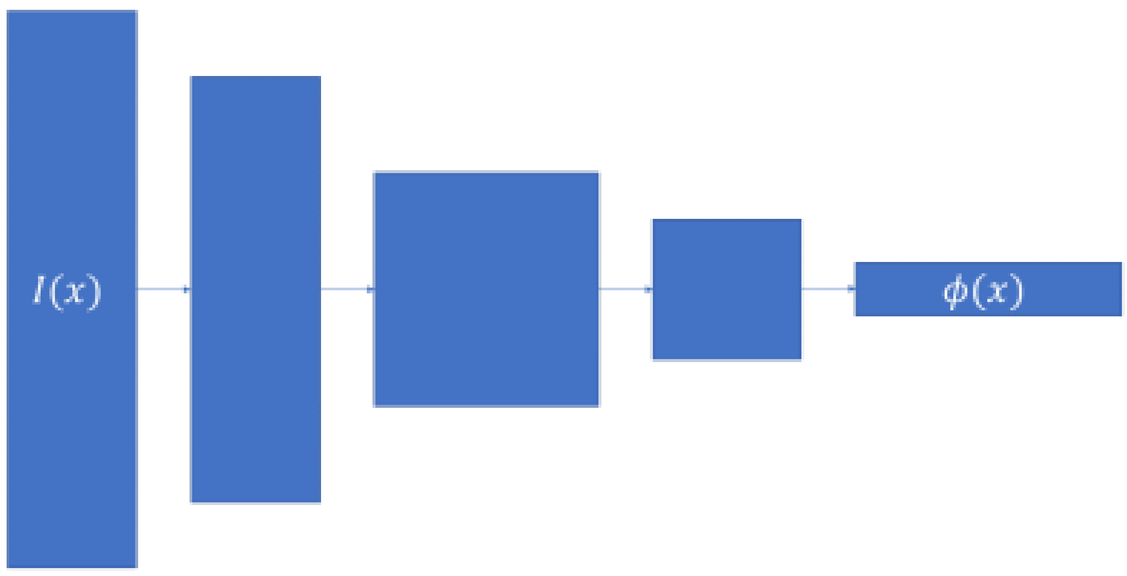
Simulated Reference Image:
Left: A real image of a toothbrush with anomaly from the dataset of MVTec. Right: A simulated reference image where the anomaly is eliminated.



Generating Simulated Reference:
CNN architecture of training and generating simulative reference image. In the training phase, we supply as input the real reference R(x) while in test time we use the defect candidate image I(x).



Generating Feature Vector:
CNN architecture of generating the representation feature vector φ(x) given an input image I(x).



Test Examples:
Prediction masks on anomalies on the toothbrush dataset of MVTEc based on simulated reference trainset applied with the Patch Core method.